SUBARRAY CONTROL AND SUBARRAY CELL ACCESS IN A MEMORY MODULE

ABSTRACT OF THE DISCLOSURE

The present invention provides a subarray control apparatus and method. The subarray control includes a wordline driver configured to generate a wordline activation signal, and a write/read control signal generator configured to generate a write/read enable signal. In addition, the subarray control includes a timing generator configured to generate a wordline timing signal input to the wordline driver and a write/read timing signal input to the write/read control signal generator. The wordline activation signal is based on enable data captured by a first transparent latching circuit and the wordline timing signal generated within the subarray. The write/read enable signal is based on enable data captured by a second transparent latching circuit and the write/read timing signal generated within the subarray. Accessing subarray cells in a memory module and a memory module incorporating the subarray control are also disclosed.